communication signals. The total number of conductive pins for the integrated circuit component is fewer than a conventional integrated circuit component for performing the same functional operation.

[039] The above paragraph illustrates how, in one embodiment, two chips may be connected on the system bus without increasing the number of system bus pins on each component, which is one advantage of this invention. With regard to FIG. 5, however, another significant reduction in pin count is realized. In this regard, a conventional memory controller component would require 4 sets of memory interconnect pins to interface the four memory busses of memories 361, 362, 363, and 364 to the system bus 305. The illustrated embodiment, as shown in FIG. 5, reduces the required memory interface pins per component by half (per chip), which will result in a significant reduction in the manufacturing cost of the component.

[040] It should be appreciated that there are a variety of ways to implement the requisite circuitry and logic for carrying out the functionality and operations described above. One such particular implementation is described and illustrated in co-pending application serial number 10/630,260, entitled "Integrated Circuit with a Scalable High-Bandwidth Architecture," and filed on July 30, 2003 ~~(and identified by attorney docket number 50833-1240)~~, which co-pending application is incorporated herein by reference.

[041] Having described certain embodiments that embody one aspect of the invention, reference will now be made to another aspect of the present invention. In this regard, reference is made to FIG. 6, which is a diagram similar to the diagram of FIG. 2. The diagram of FIG. 6, however, illustrates a system 400 having an additional chip 410 interposed between the chips 210 and 211. The chip 410 may be identical in design to the chips 210 and 211. In configuration, however, split bus logic interfaces